Higher Computing Science
Data Representation
Summary Notes

Computer architecture - Processor

The CPU (Central Processing Unit) is the main processor in a computer.
It has 3 main components:

Control Unit	manages the execution of program instructions and fetching from memory
ALU (Arithmetic and Logic Unit)	performs arithmetical operations (add, subtract, multiply, divide) and logical decisions (AND, OR, NOT)
Registers	Temporary storage locations inside the processor, used to store data, instructions & addresses **Memory Address Register** Stores the address of data currently in use by the processor **Memory Data Register** Stores the data or instruction to be processed

Computer architecture - Memory

Memory is used to store programs while they are running. It is organised into millions of individual storage locations, each with a unique binary address.

Type of Memory	Description
RAM (Random Access Memory)	Can be written to, stores program which are in use, loses its contents when power is switched off
ROM (Read Only Memory)	Can't be written to, retains contents even when power is switched off. Used to store the **bootstrap loader**, the program which loads up the OS when the computer is turned on
Cache	An area of fast access memory, physically close to the processor used to store frequently used instructions. Cache improves system performance as access time is much faster than accessing RAM. Programs working with large data structures such as parallel arrays and arrays of records will store these in cache for fast access while the program is running.

Computer architecture - Buses

Buses are sets of wires which connect the processor and memory.

- **Data bus** – caries binary data to and from memory.
- **Address bus** – carries the memory location which data is to be written to or read from.
- **Control bus** – comprises several discrete lines, including:
    - **Read line** – used to signal a memory read operation.
    - **Write line** – used to signal a memory write operation.
    - **Clock line** – carries electronic pulses to CPU to keep components synchronised.
    - **Reset line** – carries a signal which returns processor to its original state.
    - **Interrupt line** – carries a signal to processor when a peripheral requires attention

Computer architecture – Fetch-execute cycle

The way the CPU repeatedly fetches an instruction from memory, decodes it, and then executes it, is called the **fetch-execute cycle**.

Memory Read operation

1. CPU sets up the address bus with the required memory address by placing a value in the Memory Address Register.
2. The Control Unit activates the read line.
3. The contents of the storage location with that address are released on to the data bus and copied into the Memory Data Register.
4. The data is decoded and executed.

Memory Write operation

1. CPU sets up the address bus with the required memory address by placing a value in the Memory Address Register.
2. CPU sets up data bus with value to be written to memory, by placing the value in the Memory Data Register.
3. The Control Unit activates the write line.
4. The contents of the Memory Data Register are transferred to the appropriate storage location.

Computer architecture – Addressable memory

Addressable memory is the maximum amount of memory which a particular computer can actually use. Adding any more memory than this is pointless as the computer will be unable to use it.

- **Address bus width** determines how much memory can be addressed. No matter how much RAM is available, the address bus determines how much of it can actually be used.
  For example, there may be 16777216 storage locations in RAM, but a 16 bit address bus can only access 2^{16} = 65536 of them.
- The **width of the data bus** gives us the **word size** (aka word length) – the number of bits that can actually be carried to and from each storage location.
  For example, a 16 bit data bus means the computer has a word length of 16 bits.

In combination, these allow us to work out the amount of addressable memory.

Example (addressable memory)

A computer has a 32 bit data bus and a 24 bit address bus - calculate the addressable memory.

- The word size is 32 bits.
- The number of locations that can be addressed is 2^{24} = 16777216.
- The *amount* of addressable memory is therefore:
  16777216 locations x 32 bits = 536870912 bits
  = 67108864 bytes
  = 65536 Kb
  = 64 Mb of addressable memory.